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(54) Tunneling emitters and method of making

(57) An emitter (100) has an electron supply layer (10) and a tunneling layer (20) formed on the electron supply layer. Optionally, an insulator layer (78) is formed on the electron supply layer and has openings defined within in which the tunneling layer is formed. A cathode layer (14) is formed on the tunneling layer. A conductive layer (82) is partially disposed on the cathode layer and partially on the insulator layer if present. The conductive layer defines an opening to provide a surface for energy emissions (22) of electrons (16) and/or photons (18). Preferably but optionally, the emitter is subjected to an annealing process (120,122) thereby increasing the supply of electrons tunneled from the electron supply layer to the cathode layer.

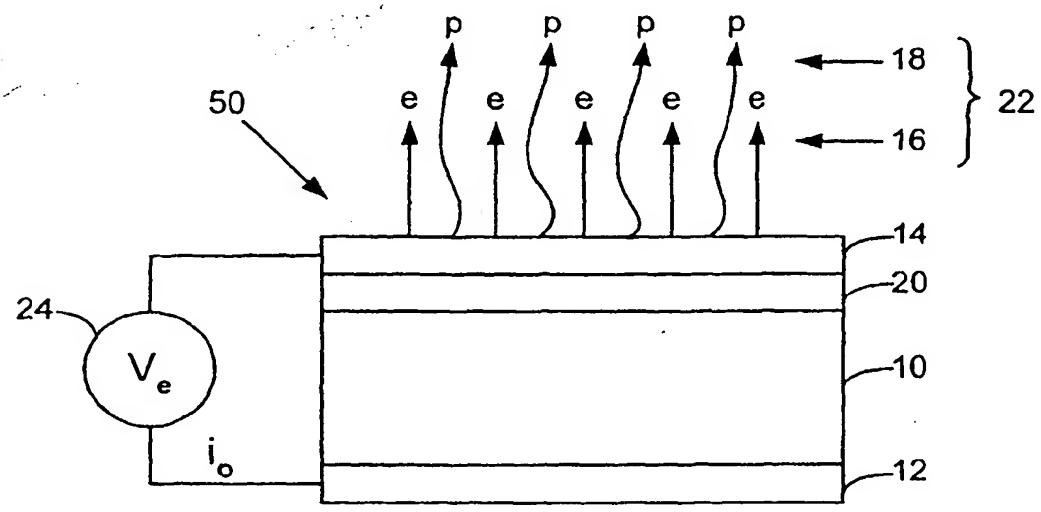

Fig. 1

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Description

FIELD OF THE INVENTION

[0001] The invention is directed to field emission devices. In particular the invention is directed to flat field emission emitters utilizing tunneling and their use in electronic devices.

BACKGROUND OF THE INVENTION

[0002] Several different field emission devices have been proposed and implemented to create electron emissions useful for displays or other electronic devices such as storage devices. Traditionally, vacuum devices with thermionic emission such as electron tubes required the heating of cathode surfaces to create electron emission. The electrons are drawn in a vacuum space to an anode structure that is at a predetermined voltage potential which attracts the electrons. For a display device such as a cathode ray tube, the anode structure is coated with phosphors such that when an electron impinges on the phosphor, photons are generated thereby creating a visible image. Cold cathode devices such as spindt tips (pointed tips) have been used or proposed to replace the hot cathode technology in some applications. However, it has been difficult to reduce the size and integrate several spindt tips while maintaining reliability. As the size is reduced, the spindt tip becomes more susceptible to damage from contaminants in the vacuum that are ionized when an electron strikes it. The ionized contaminant is then attracted to the spindt tip and collides with it, thereby causing damage. To increase the life of the spindt tip, the vacuum space must have an increasingly high vacuum. A flat emitter having a larger emission surface can be operated reliably at lower vacuum requirements. However, for some applications, the amount of current density from conventional flat emitters is not high enough to be useful. Thus a need exists to create a flat emitter that has high-energy current density that is also able to operate reliably in low vacuum environments.

SUMMARY

[0003] An emitter has an electron supply layer and a tunneling layer formed on the electron supply layer. Optionally, an insulator layer is formed on the electron supply layer and has openings defined within in which the tunneling layer is formed. A cathode layer is formed on the tunneling layer. A conductive layer is partially disposed on the cathode layer and partially on the insulator layer if present. The conductive layer defines an opening to provide a surface for energy emissions of electrons and/or photons. Preferably but optionally, the emitter is subjected to an annealing process thereby increasing the supply of electrons tunneled from the electron supply layer to the cathode layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The invention is better understood with reference to the following drawings. The elements of the drawings are not necessarily to scale relative to each other. Rather, emphasis has instead been placed upon clearly illustrating the invention. Furthermore, like reference numerals designate corresponding similar parts through the several views.

[0005] Fig. 1 is an exemplary illustration of a tunneling emitter incorporating the invention.

[0006] Fig. 2 is an exemplary illustration of the use of the tunneling emitter of Fig. 1 to create a focused electron beam.

[0007] Fig. 3 is an exemplary illustration of an integrated circuit that includes several tunneling emitters and an optical lens to create a display device.

[0008] Fig. 4 is an exemplary block diagram of an integrated circuit that incorporates multiple tunneling emitters and control circuitry.

[0009] Fig. 5 is an exemplary illustration of a tunneling emitter on an integrated circuit that includes a lens for focusing the energy emissions from the tunneling emitter.

[0010] Fig. 6 is an exemplary display that is created from an integrated circuit that includes multiple tunneling emitters and an anode structure that creates or passes photons.

[0011] Fig. 7A is an exemplary storage device that incorporates an integrated circuit that includes multiple tunneling emitters for reading and recording information onto a rewriteable media.

[0012] Fig. 7B is a schematic of an exemplary read circuit incorporated into the exemplary storage device of Fig. 7A.

[0013] Fig. 8 is a top view of an exemplary tunneling emitter.

[0014] Fig. 9 is an exemplary cross-sectional view of the tunneling emitter shown in Fig. 8.

[0015] Fig. 10 is an exemplary block diagram of a computer that incorporates at least one of the electronic devices, a display or storage device, which incorporate the tunneling emitters of the invention.

[0016] Figs. 11A-11J are illustrations of exemplary steps used in a first exemplary process to create the tunneling emitter of the invention.

[0017] Figs. 12A-12D are illustrations of exemplary steps used in a second exemplary process to create the tunneling emitter of the invention.

[0018] Figs 13A and 13B are charts of exemplary annealing processes used to optionally improve the tunneling emitters of the invention.

DETAILED DESCRIPTION OF THE PREFERRED AND ALTERNATE EMBODIMENTS

[0019] The present invention is directed to field emission emitters that provide high levels of emission current

per square centimeter by using a tunneling layer that has a sufficient thinness between about 50 and about 5000 Angstroms to create an electric field between an electron source and a flat cathode surface. Conventional flat emitter type devices have low emission current per square centimeter of surface area and thus are not usable in several applications. The invention uses a thin deposition of either a silicon-based dielectric having suitable defects, a metal cluster dielectric having high dielectric strength for direct tunneling, or other tunneling material, to create a barrier in which electrons can tunnel between the electron source and the cathode surface preferably directly or through the defects within the dielectric. By using such material, the emission current can be greater than 10 mAmps, 100 mAmps, or 1 Amp per square centimeter which is one, two, or three orders of magnitude, respectively, greater than that of conventional flat emitter technology. The actual emission rate will depend upon the design choices of the type and thickness of material used for the tunneling layer. In addition to electron emissions, the invention is also able to create photon emissions that provides for additional uses for the emitter incorporating the invention. Further advantages and features of the invention will become more apparent in the following description of the invention, its method of making and various applications of use.

[0020] In the illustrations of this description, various parts of the emitter elements have not been drawn to scale. Certain dimensions have been exaggerated in relation to other dimensions in order to provide a clearer illustration and understanding of the present invention. For the purposes of illustration, the embodiments illustrated herein are shown in two-dimensional views with various regions having depth and width. It should be understood that these region are illustrations only of a portion of a single cell of a device, which may include a plurality of such cells arranged in three-dimensional structures. Accordingly, these regions will have three dimensions, including length, width, and depth when fabricated on an actual device.

[0021] Further, one aspect of the invention is that it can be fabricated using conventional integrated circuit thin-film technologies. Several different technologies exist to perform several of the process steps and can be interchanged by those having skill in the art. For example, deposition of material can be by one of several processes such as evaporation, sputtering, chemical vapor deposition, molecular beam epitaxy, photochemical vapor deposition, low temperature photochemical vapor deposition, and plasma deposition, to name a few. Additionally, several different etch technologies exist such as wet etching, dry etching, ion beam etching, reactive ion etching, and plasma etching such as barrel plasma etching and planar plasma etching to name some of the possible etching technologies. Choice of actual technologies used will depend on material used and cost criteria among other factors.

[0022] Fig. 1 is an exemplary diagram of an emitter device 50, preferably a flat emitter for electron and photon emission, which includes an electron source 10. On the electron source 10 is a tunneling layer 20. Preferably, the tunneling layer 20 is formed from a metal cluster dielectric or a silicon-based dielectric. Exemplary metal cluster dielectrics include tungsten silicon nitrate (WSiN) or tantalum oxide (Tao,), titanium oxide (TiO_x, where x = 0.5 to 2.5). Also, tantalum aluminum oxynitride ($TaAlO_xN_y$), tantalum aluminum oxide ($TaAlO_x$), aluminum oxynitride (AlO_xN_y) or other transitionary metal (TM) oxides or oxynitrides ($(TM)O_x$ or $(TM)O_xN_y$) are envisioned as being capable of use as tunneling layer 20. A metal cluster dielectric tunneling layer preferably has a thickness less than 500 Angstroms and more preferably the thickness is within the range of about 50 to about 250 Angstroms, such as 100 Angstroms or less. Exemplary silicon-based dielectrics are SiN_x, Si_3N_4 (RI~2.0),Si_xN_y(x:y> ¾, RI~2.3), and SiC. Also, F_y-SiO_x and C_y-SiO_x are envisioned as being capable of use as tunneling layer 20. The silicon-based dielectric layer preferably has a thickness about 500 Angstroms and more preferably the thickness is within the range of about 250 to about 5000 Angstroms, such as 500 Angstroms or less. The chosen thickness determines the electrical field strength that the tunneling layer 20 must be able to withstand and the desired emitter emission current. Disposed on the tunneling layer 20 is a cathode layer 14, preferably a thin-film conductor such as platinum, gold, molybdenum, iridium, ruthenium, tantalum, chromium, or other refractive metals or alloys thereof. Other cathode layers can be used and are known to those skilled in the art. Preferably, the thickness of the cathode layer is 30 to 150 Angstroms. When a voltage source 24 having an emitter voltage V_e (about 3-20V) is applied to the cathode layer 14 and electron supply 10 via a contact 12, electrons tunnel directly or indirectly from the substrate 10 (an electron supply) to the cathode layer 14. When there are defects within the tunneling layer 20, the electric field in which the electrons tunnel through is punctuated with various gaps and the electron emission 16 from the surface of the cathode layer 14 is greater than conventional designs. Alternatively, if the dielectric is thin enough, direct tunneling occurs. Also, some photon emission 18 occurs along with the electron emission 16 to form the energy emission 22 from the emitter 50.

[0023] The electron field is calculated for various thicknesses as $\vec{E} = \frac{V_e}{t_{thickness}}$ where $t_{thickness}$ is the thickness of tunneling layer 20. For example, for a V_e=10V, the electric field is equal to 2×10^6 volts/meter for a 500 Angstrom thickness in the tunneling layer 20. The minimum thickness for a particular dielectric will depend on its dielectric strength.

[0024] Preferably, a metal cluster dielectric tunneling layer 20 is sputter deposited. By using metal cluster dielectrics as the tunneling layer, very high electric field strength can be applied between the electron source 10 and the cathode layer 14 to achieve higher emission,

because the metal cluster dielectrics withstand much higher electrical field strength without electrical breakdown. Metal cluster dielectrics allow for direct tunneling to occur.

[0025] Preferably, a silicon-based dielectric tunneling layer 20 is deposited using plasma enhanced chemical vapor deposition (PECVD). By using silicon-based dielectrics as the tunneling layer, defective areas throughout the material are achieved and tunneling is done through the various defects due to the electric field generated between the electron source 10 and the cathode layer 14.

[0026] Fig. 2 is an exemplary diagram of a use for the emitter 50 of Fig. 1. In this application, the electron emission 16 is focused by an electrostatic focusing device or lens 28, exemplified as an aperture in a conductor that is set at predetermined voltage that can be adjusted to change the focusing effect of the lens 28. Those skilled in the art will appreciate that lens 28 can be made from more than one conductor layer to create a desired focusing effect. The electron emission 16 is focused by lens 28 into a focused beam 32 onto an anode structure 30. The anode structure 30 is set at an anode voltage V_a 26 which magnitude varies for an application depending on the intended use and the distance from the anode structure 30 to the emitter 50. For instance, with anode structure 30 being a recordable medium for a storage device, V_a might be chosen to be between 500 and 1000 Volts. The lens 28 focuses the electron emission 16 by forming an electric field 34 within its aperture. By being set at a proper voltage from $V_,$, the electrons emitted from the emitter 50 are directed to the center of the aperture and then further attracted to the anode structure 30 to form the focused beam 32.

[0027] Fig. 3 is an exemplary embodiment of a display 40 having an integrated circuit 52 that includes multiple integrated emitters 100 formed in an array of pixel groups. The integrated emitters 100 emit photon emission 18, a visible light source, which is focused with an optical lens 38 to a focused beam 32 that is viewable as an image. Preferably, the optical lens 38 is coated with a transparent conducting surface, such as indium tin oxide, to capture electrons emitted from the emitter.

[0028] Fig. 4 is an exemplary embodiment of an integrated circuit 52 that includes at least one integrated emitter 100 but preferably a plurality of integrated emitters 100 arraigned in an array. An emitter control circuit 72 is integrated onto the integrated circuit 52 and used to operate the at least one integrated emitter 100.

[0029] Fig. 5 is an exemplary embodiment of an integrated circuit 52 that includes an integrated emitter 100 and a lens array 48. The integrated circuit 52 is formed on a conductive substrate 10, preferably heavily doped silicon or a conductive material such as a thin film conductive layer to provide an electron source. On the substrate 10 is disposed a tunneling layer 20 having a thickness between about 50 Angstroms and about 5000 Angstroms, preferably about 100 Angstroms although about 50 to about 750 Angstroms is further preferable for some applications and materials. Different layers of semiconductor thin-film materials are applied to the substrate 10 and etched to form the integrated emitter 100. Disposed on the tunneling layer 20 is a cathode layer 14, preferably a thin-film conductive layer of platinum, gold, molybdenum, iridium, ruthenium, tantalum, chromium, or other refractive metals or alloys thereof. The cathode layer 14 forms a cathode surface from which energy in the form of electrons and photons are emitted. The lens array 48 is applied using conventional thin-film processing and includes a lens 28 defined within a conductive layer and aligned with the integrated emitter 100 to focus the energy from the integrated emitter 100 onto a surface of an anode structure 76. Anode structure 76 is located a target distance 74 from the integrated circuit 52.

[0030] Fig. 6 is an alternative embodiment of a display application using the integrated emitter 100 of the invention. In this embodiment, a plurality of emitters 100 is arranged and formed in an integrated circuit 52. Each of the emitters 100 emits energy emission 22 in the form of electron emissions 16 or photon emissions 18 (see Fig. 1). An anode structure, display 40, receives the emitted energy in display pixel 44, made up of display sub-pixels 42. Display sub-pixel 42 is preferably a phosphor material that creates photons when struck by the electron emission 16 of energy emission 22. Alternatively, display sub-pixel 42 can be a translucent opening to allow photon emission 18 of energy emission 22 to pass through the display 40 for direct photon viewing.

[0031] Fig. 7A is an alternative use of an integrated emitter 100 within in a storage device. In this exemplary embodiment, an integrated circuit (IC) 52 having a plurality of integrated emitters 100 has a lens array 48 of focusing mechanisms aligned with integrated emitters 100. The lens array 48 is used to create a focused beam 32 that is used to affect a recording surface, media 58. Media 58 is applied to a mover 56 that positions the media 58 with respect to the integrated emitters 100 on IC 52. Preferably, the mover 56 has a reader circuit 62 integrated within.

[0032] In Fig. 7B, the reader 62 is shown as an amplifier 68 making a first ohmic contact 64 to media 58 and a second ohmic contact 66 to mover 56, preferably a semiconductor or conductor substrate. When a focused beam 32 strikes the media 58, if the current density of the focused beam is high enough, the media is phase-changed to create an effected media area 60. When a low current density focused beam 32 is applied to the media 58 surface, different rates of current flow are detected by amplifier 68 to create reader output 70. Thus, by affecting the media with the energy from the integrated emitter 100, information is stored in the media using structural phase changed properties of the media. One such phase-change material is In_2Se_3. Other phase change materials are known to those skilled in the art such as chalcogenide alloys, for example: GaSb, InSb, InSe, Sb_2Te_3, $Ge_2Sb_2Te_5$, InSbTe, GaSeTe,

$SnSb_2Te_4$, InSbGe, AgInSbTe, (GeSn)SbTe, GeSb (SeTe), $Te_{81}Ge_{15}Sb_2S_2$, and GeSbTe.

[0033] Fig. 8 is a top view of an exemplary embodiment of the invention of an integrated emitter 100 that includes an emitter area 84 within the cathode layer 14. The cathode layer 14 is electrically coupled to and disposed beneath conductive layer 82 that is further partially disposed over insulator layer 78. Integrated emitter 100 is shown as preferably a circular shape, however other shapes can be used. The circular shape is preferable in that the electric fields generated are more uniform as there are no discrete edges within the shape which may affect the electric field strength.

[0034] Fig. 9 is a cross-section of the exemplary embodiment of integrated emitter 100 shown in Fig. 8 looking into the 9-9 axis. A substrate 10, preferably a conductive layer or a highly doped semiconductor provides an electron supply to tunneling layer 20 that is disposed within an opening defined within an insulator layer 78 and partially over the surface of insulator layer 78. A cathode layer 14, preferably a thin-film conductive layer is disposed over the tunneling layer 20 and partially beneath the conductive layer 82 thereby making electrical contact with the conductive layer. Optionally, an adhesion layer, such as tantalum, can be applied before conductive layer 82 to provide for a bonding interface between the conductive layer 82 and the insulator layer 78 depending on the particular materials chosen for insulator layer 78 and conductive layer 82.

[0035] Fig. 10 is an exemplary block diagram of a computer 90 that includes a microprocessor 96, memory 98, which is coupled to the microprocessor 96, and electronic devices, a storage device 94 and a display device 92. The electronic devices are coupled to the microprocessor 96. The microprocessor 96 is capable of executing instructions from the memory to allow for the transfer of data between the memory and the electronic devices, such as the storage device 94 and the display device 92. Each electronic device includes an integrated circuit that has an emitter incorporating the invention and preferably a focusing device for focusing the emissions from the emitter. The emitter has an electron supply layer with an insulating layer disposed thereon. The insulating layer has an opening defined within which a tunneling layer is formed on the electron supply layer. On the tunneling layer is a cathode layer. Preferably but optionally, the integrated circuit with the emitter has been subjected to an annealing process thereby increasing the supply of electrons that can tunnel from the electron supply layer to the cathode layer.

[0036] Figs 11A to 11J illustrate exemplary process steps used to create an emitter incorporating the invention. In Fig 11 A, a mask 102, of dielectrics or photoresist is applied to a substrate 10, preferably a silicon semiconductor substrate, although substrate 10 might be a conductive thin-film layer or a conductive substrate. Preferably substrate 10 has a sheet resistance of about 100 to 0.0001 ohms centimeter.

[0037] In Fig. 11B an insulator layer 78 is created, preferably by field oxide (FOX) growth when substrate 10 is a silicon substrate. Optionally, the insulator layer 78 can be formed of other oxide, nitride, or other conventional dielectrics deposited or grown alone or in combination using conventional semiconductor processes. The insulator layer 78 is created on substrate 10 except in areas covered by mask 102. The area defined by mask 102, and thus the resulting voids or defined openings within insulator layer 78 determines the location and shape of the latter formed integrated emitter 100 when mask 102 is removed.

[0038] In Fig. 11C, a tunneling layer 20 is applied on the substrate 10 and insulator layer 78. Preferably, a silicon-based dielectric used as tunneling layer 20 is applied using plasma enhanced chemical vapor deposition (PECVD). Other deposition techniques are known to those skilled in the art. The tunneling layer 20 is preferably SiC, SiN_x, Si_3N_4 (RI ~ 2.0), or Si_xN_y (x:y >3/4, RI -2.3). Optionally, F_y-SiO_x and C_y-SiO_x are envisioned as suitable material for tunneling layer 20. The silicon-based dielectric used as tunneling layer 20 is preferably about 250 to about 5000 Angstroms thick.

[0039] Optionally, a tunneling layer 20 of preferably a high dielectric strength material such as metal cluster dielectrics, TiO_x, TaO_x, WSiN, $TaAlO_xN_y$, $TaAlO_x$ or AlO_xN_y, but preferably TiO_x, is applied over the surface of the processed substrate 10 and insulator layer 78. The metal cluster dielectric used tunneling layer 20 is preferably deposited by sputtering metal and introducing oxygen and/or nitrogen to form the dielectric to a thickness of less than about 500 Angstroms, preferably between about 50 to about 250 Angstroms, such as about 100 Angstroms.

[0040] Although two types of tunneling materials have been illustrated, other tunneling materials can be used to provide the tunneling layer 20 and still meet the spirit and scope of the invention.

[0041] After tunneling layer 20 has been deposited a cathode layer 14 is deposited, sputtered or otherwise applied onto the tunneling layer 20. Fig. 11C shows the result of the application of a cathode layer 14 over the surface of the processed substrate 10. The cathode layer 14 is preferably a thin-film metallic layer such as platinum or gold and preferably has a thickness of about 50 to about 250 Angstroms. Other metals can be used for cathode layer 14 such as molybdenum, iridium, ruthenium, tantalum, chromium, or other refractive metals or alloys thereof, to name a few. The cathode layer 14 disposed on tunneling layer 20 within the opening of insulator layer 78 forms the emitter surface 86

[0042] Fig. 11D shows the applying of an etch photomask 55 disposed over the emitter surface 86 and partially over the insulator layer 78 to define the shape and location of the emitter structure. Fig. 11E shows the result of an etch of the cathode layer 14 and the tunneling layer 20.

[0043] Fig. 11F shows the applying of a first photore-

sist layer 57 after etch photomask 55 has been stripped and a second photoresist layer 59 on the processed substrate 10 used to create a reentrant profile. Preferably, first photoresist layer 57 is a thick coat of resist that has photoactive compound (PAC) that is stable at very high temperatures (i.e. greater than about 130C). After the first photoresist layer 57 is applied it is preferably soft baked. Then the first photoresist layer 57 is flood exposed at an energy level depending on the type of etch profile required. The first photoresist layer 57 is then hard baked at about 120C to about 150C for 90 to 180 seconds on a hot plate.

[0044] The second photoresist layer 59 is applied preferably in a thin coat by either spinning or deposition on top of the first photoresist layer 57 and then baked at about 90 to about 110C for about 60 seconds. The baking of the second photoresist layer 59 redistributes its PAC into the first photoresist layer to create a variable density of PAC photoresist layer 61.

[0045] In Fig. 11G, a photomask 63 is applied on the surface of the variable density photoresist layer 61 to define the emitter shape and location.

[0046] In Fig. 11H, the variable density photoresist layer 61 is developed in TMAH (tetramethyl ammonium hydroxide) based developer or other for about 20 to about 60 seconds depending on the applied thickness. This developing process creates a highly re-entrant profile useful in preventing further deposited metal from adhering to the walls of the etched opening. Conventional processes allow deposited metal to form on near vertical or non-reentrant sidewalls. This sidewall deposited metal creates problems in that the metal on the sidewall can lead to pieces that remain on the processed substrate and cause shorts or contamination. Also, it is difficult to etch a metal trace and stop on thin metal.

[0047] Alternative methods for creating the re-entrant side wall profile include modifying the exposure energy during the flood exposure stage, using dyed/undyed resist, using high/low contrast resist, and controlling the relative dissolution rate of the first photoresist layer 57 and the second photoresist layer 59 in developer by controlling the solvent and PAC in the first photoresist layer 57 using post-flood exposure bake conditions such as temperature and time. The basic theory used is to create an appropriate gradient of PAC in the positive photoresist. The resist is then exposed to radiation and developed. The rate of dissolution of resist is inversely proportional to the PAC concentration and hence can create a non-vertical side wall profile such as the re-entrant structure shown.

[0048] In Fig. 11I, the photomask 63 has been preferably stripped and conductive layer 82 deposited or sputtered onto the processed substrate 10. Before applying the conductive layer 82 an optional adhesive layer is applied first to increase the adhesion to insulator layer 78. The optional adhesive layer is preferably tantalum when the later applied conductive layer 82 is gold. Preferably, the adhesive layer is applied using conventional deposition techniques. The adhesive layer is preferably up to about 200 Angstroms thick. The conductive layer 82 is applied on the previously applied layers on substrate 10, such as the adhesive layer if used. Preferably, the conductive layer 82 is formed using conventional deposition techniques. The conductive layer is preferably gold that is about 500 to about 1000 Angstroms thick.

[0049] In Fig. 11J a lift-off process is used to remove variable density photoresist layer 61 and the portion of conductive layer 82 that is disposed on it to create the emitter device 50. Preferably, low temperature plasma is used to reactively etch ash organic materials within the variable density photoresist layer 61. The gas used is preferably oxygen in a planer plasma etch process. The processed substrate 10 is placed in a chamber and the oxygen is introduced and excited by an energy source to create a plasma field. The plasma field energizes the oxygen to a high energy state, which, in turn oxidizes the variable density photoresist layer 61 components to gases that are removed from the chamber by a vacuum pump

[0050] Optionally, a wet lift-off process can be used in lieu of the plasma lift-off process. The processed substrate 10 is immersed in a solvent with megasonic or ultrasonic agitation that will swell and remove the variable density photoresist layer 61 and that portion of conductive layer 82 that is disposed on it.

[0051] Figs 12A-12D illustrate exemplary alternative process steps to those shown in Figs. 11A-11J that can be used to create an alternative emitter device 50'. In Fig. 12A, a protective layer 65 is applied after application of the cathode layer 14. Preferably the protective layer 65 is a layer of titanium or molybdenum and is used to prevent contamination of the emitter surface 86 on cathode layer 14 during further processing. The variable density photoresist layer 61 is applied on the surface of the processed substrate 10 and patterned and exposed with photomask 63.

[0052] Fig. 12B illustrates the results of etching the variable density photoresist layer 61 to form a highly re-entrant profile.

[0053] Fig. 12C illustrate the application of an adhesion layer 80, such as tantalum, and the conductive layer 82, such as gold, to the processed substrate 10. Because the sidewalls of the etched variable density photoresist layer 61 are highly re-entrant, neither the adhesion layer 80 or the conductive layer 82 are deposited on the sidewalls.

[0054] Fig. 12D illustrates the result of using a lift-off process to remove the variable density layer 61 and the adhesive layer 80 and conductive layer 82 portions that are disposed on it. The alternative emitter device 50'is then selectively etched to remove the protective layer 65 to expose the emitter area 84.

[0055] By using integrated circuit thin film technology to fabricate the emitter, it can be integrated along with traditional active circuits found on conventional integrated circuits. The integrated circuit with the emitter can be

used in display devices or storage devices as previously described. Preferably, after fabrication, the emitter is subjected to an annealing process to increase the amount of emission from the emitter.

[0056] Fig. 13A and 13B are charts of exemplary annealing processes which are used to increase the emission current capability of an emitter embodying the invention. The annealing process also increases the device yields and quality by allowing the emitters to last longer. The annealing process, among other benefits, helps to decrease the resistance of contacts of dissimilar metals thereby increasing the current flow to the emitters.

[0057] In Fig. 13A, a first thermal profile 120 shows the processed substrate that includes an emitter incorporating the invention first elevated to a temperature of about 400 C within 10 minutes then held at this temperature for 30 minutes. Then the processed substrate is slowly cooled back to room temperature (about 25 C) over a period of about 55 minutes. In Fig. 13B, a second thermal profile 122 shows the processed substrate including an emitter incorporating the invention heated to a temperature of about 600 C within 10 minutes and held at that temperature for about 30 minutes. Then, the processed substrate is gradually cooled to room temperature over a period of about 100 minutes. Those skilled in the art will appreciate that the elevated temperature and the rate of cooling can be modified from the exemplary processes described and still meet the spirit and scope of the invention. By annealing the substrate that includes at least one emitter incorporating the invention, several characteristics of the emitter are improved.

[0058] It should be noted that it would be obvious to those skilled in the art that many variations and modifications may be made to the disclosed embodiments without substantially departing from the invention. All such variations and modifications are intended to be included herein within the scope of the present invention, as set forth in the following claims.

Claims

1. An emitter (100), comprising:

   an electron supply (10);
   a tunneling layer (20) disposed on the electron supply; and
   a cathode layer (14) disposed on the tunnel layer;
   a conduction layer (82) disposed partially on the cathode layer and defining an opening to create an emission area.

   wherein the electron supply, tunneling layer, and cathode layer have been subjected to an annealing process (120, 122).

2. The emitter (100) of claim 1 operable to provide an emitted energy (22) with an emission current of greater than 1 x 10^{-2} Amps per square centimeter.

3. An electronic device, comprising:

   the emitter (100) of claim 1 capable of emitting energy (22); and
   an anode structure (30, 40, 58, 76) capable of receiving the emitted energy and generating at least a first effect in response to receiving the emitted energy and a second effect in response to not receiving the emitted energy.

4. A storage device, comprising:

   at least one emitter (100) of claim 1 to generate an electron beam;
   a lens (28) for focusing the electron beam to create a focused beam (32); and
   a storage medium (58) in close proximity to the at least one emitter, the storage medium having a storage area being in one of a plurality of states (60) to represent the information stored in that storage area;

   such that:

   an effect is generated when the focused beam strikes the storage area;
   the magnitude of the effect depends on the state of the storage area; and
   the information stored in the storage area is read by measuring the magnitude of the effect.

5. An emitter (100), comprising:

   an electron supply layer (10);
   an insulator layer (78) formed on the electron supply layer and having an opening defined within;
   a tunneling layer (20) formed on the electron supply layer in the opening and further disposed over the insulator layer;
   a cathode layer (14) formed on the tunneling layer; and
   a conductive layer (82) partial disposed on the cathode layer and partially disposed on the insulator layer;

   wherein the emitter has been subjected to an annealing process (120,122) to increase the supply of electrons tunneled from the electron supply layer to the cathode layer for energy emission.

6. A method for creating an emitter (100) on an electron supply (10), comprising the steps of:

applying a tunneling layer (20) on an electron source;
applying a cathode layer (14) on the tunneling layer;
applying a variable density photoresist layer (61) over the cathode layer; and
developing the variable density photoresist layer to create a re-entrant profile of the etched openings exposing a portion of the cathode layer; and
applying a conductive layer (82) within the developed openings on the cathode layer.

7. The method of claim 6 wherein the step of applying a conductive layer (82) further includes the step of applying an adhesive layer (80) before applying the conductive layer.

8. The method of claim 6 wherein the step of applying the cathode layer (14) further comprises the step of applying a protective layer (65) over the cathode layer before the step of applying the variable density photoresist layer.

9. A method for creating an emitter (100) on an electron supply (10), comprising the steps of:

applying a tunneling layer (20) over an insulating layer (78) disposed on the electron supply, the insulator layer defining an opening to the electron supply;
applying a cathode layer (14) to adhere to the tunneling layer;
applying a variable density photoresist layer (61) on the cathode layer and insulating layer;
creating an opening in the variable density photoresist layer to the cathode layer; and
lifting off the variable density photoresist layer to remove it from the cathode layer and insulating layer.

10. A method for creating an emitter (100) on an electron supply surface (10), the method comprising the steps of:

creating an insulator layer (78) on the electron supply surface;
defining an emission area within the insulator layer;
applying a tunneling layer (20) over the insulator layer and the opening;
applying a cathode layer (14) over the tunneling layer;
etching the cathode and tunneling layers;
applying a variable density photoresist layer (61) on the cathode layer and insulator layer;
developing the variable density photoresist layer to create re-entrant openings exposing a portion of the cathode layer.
applying a conduction layer (82) on the variable density photoresist layer and within the re-entrant openings onto the cathode layer; and
lifting off the variable density photoresist layer and the conduction layer disposed upon it.

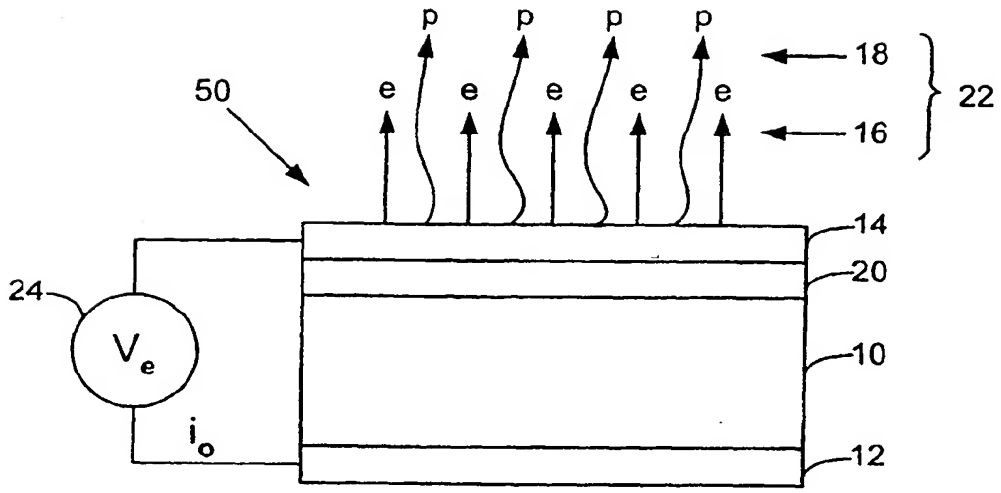

Fig. 1

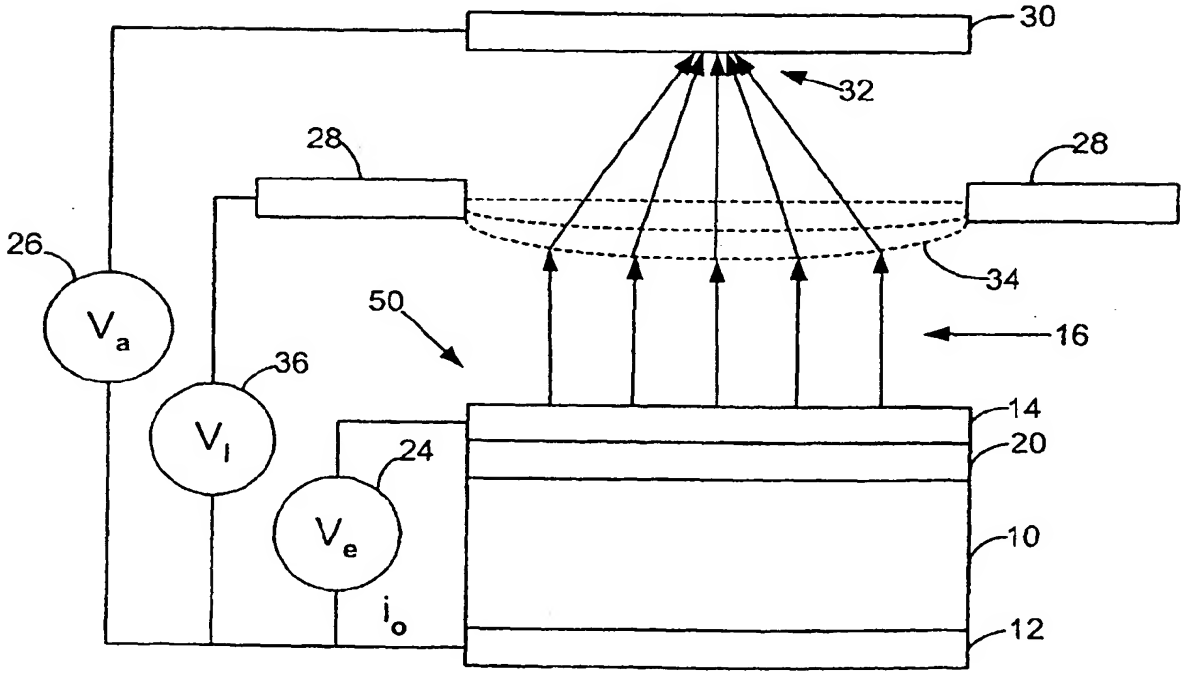

Fig. 2

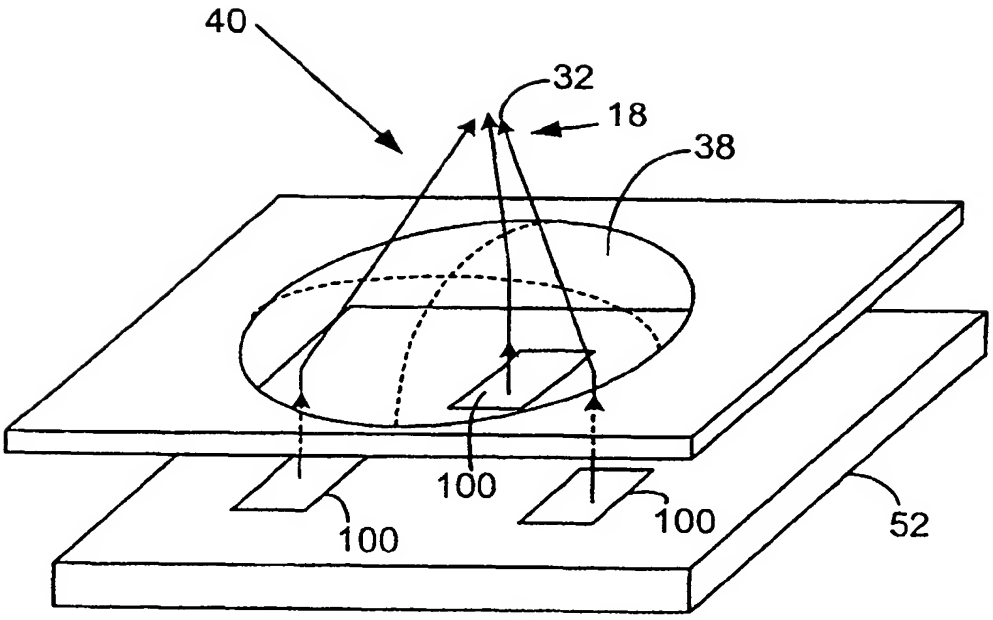

Fig. 3

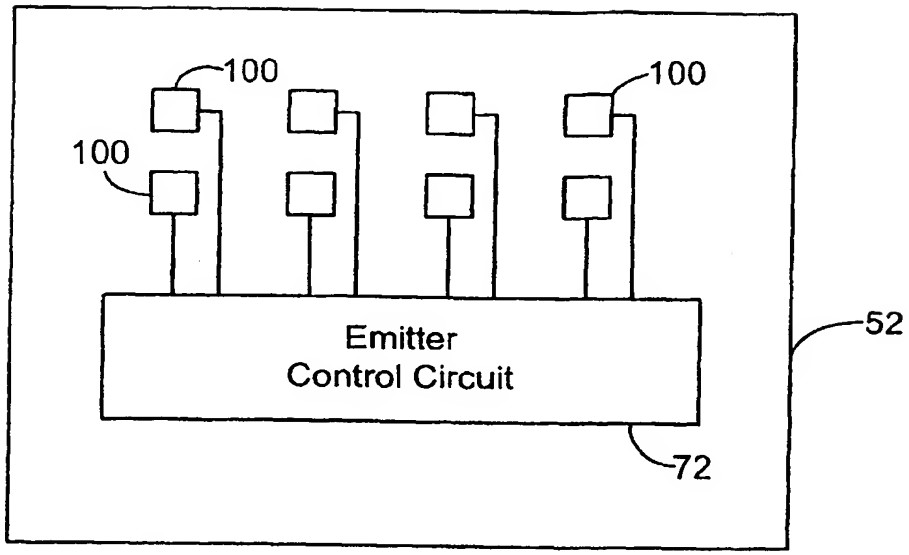

Fig. 4

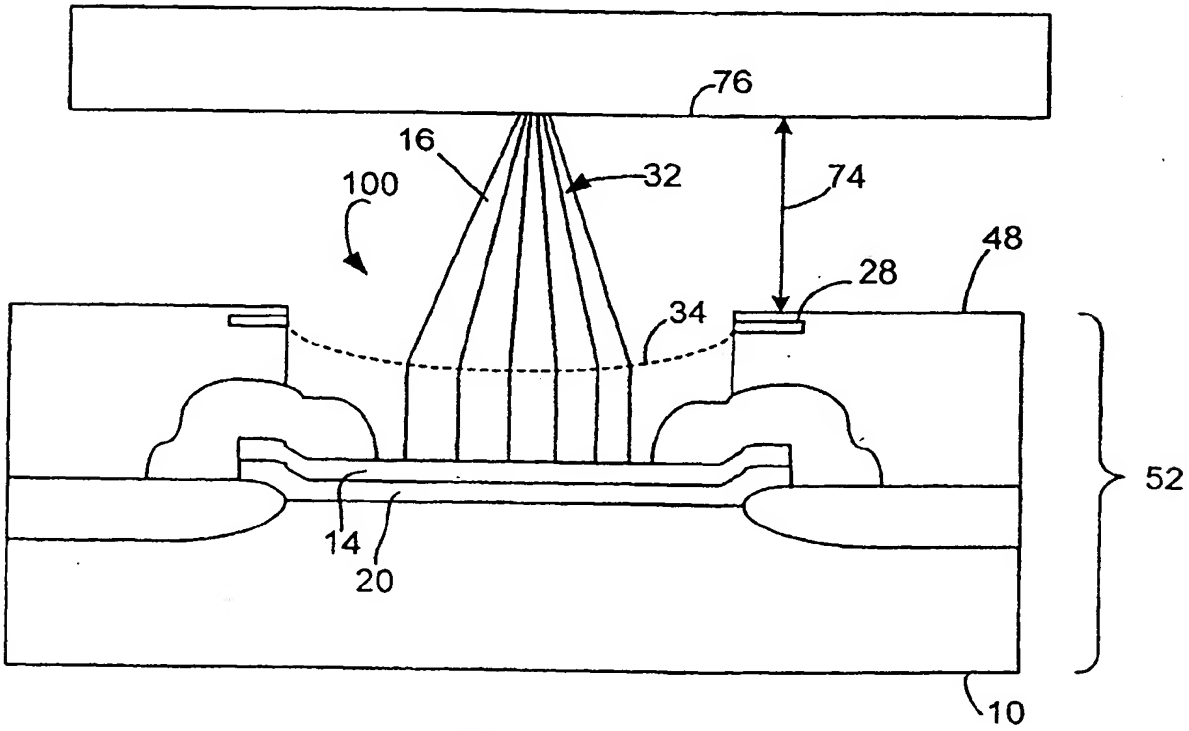

Fig. 5

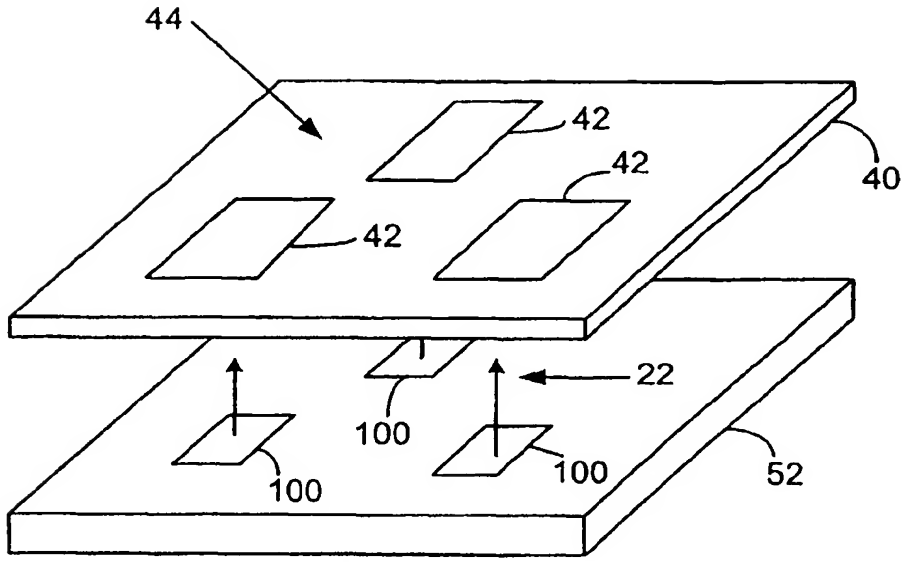

Fig. 6

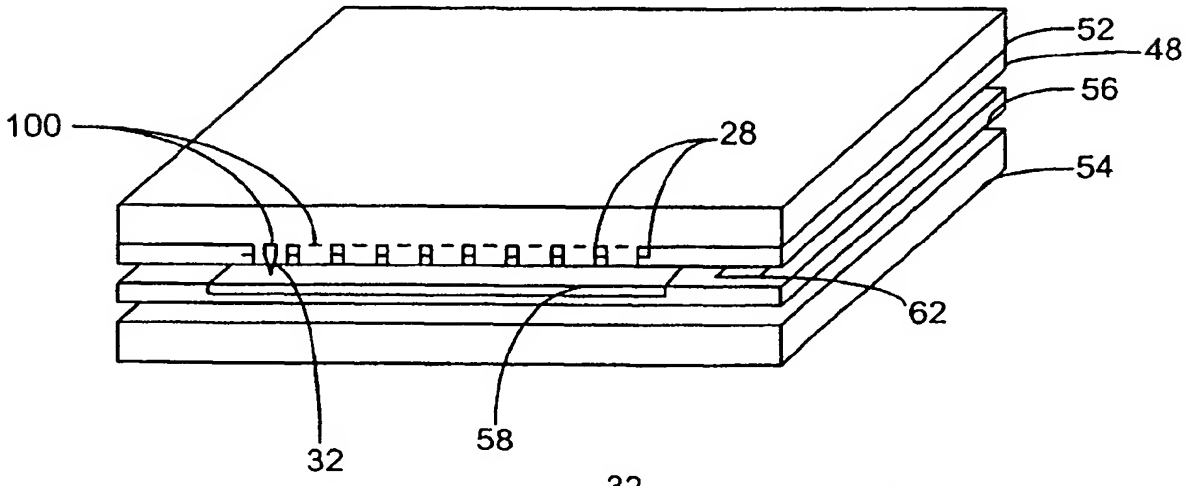

Fig. 7A

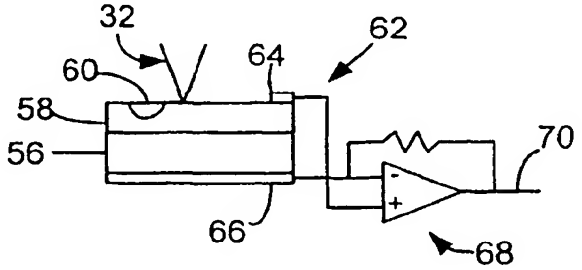

Fig. 7B

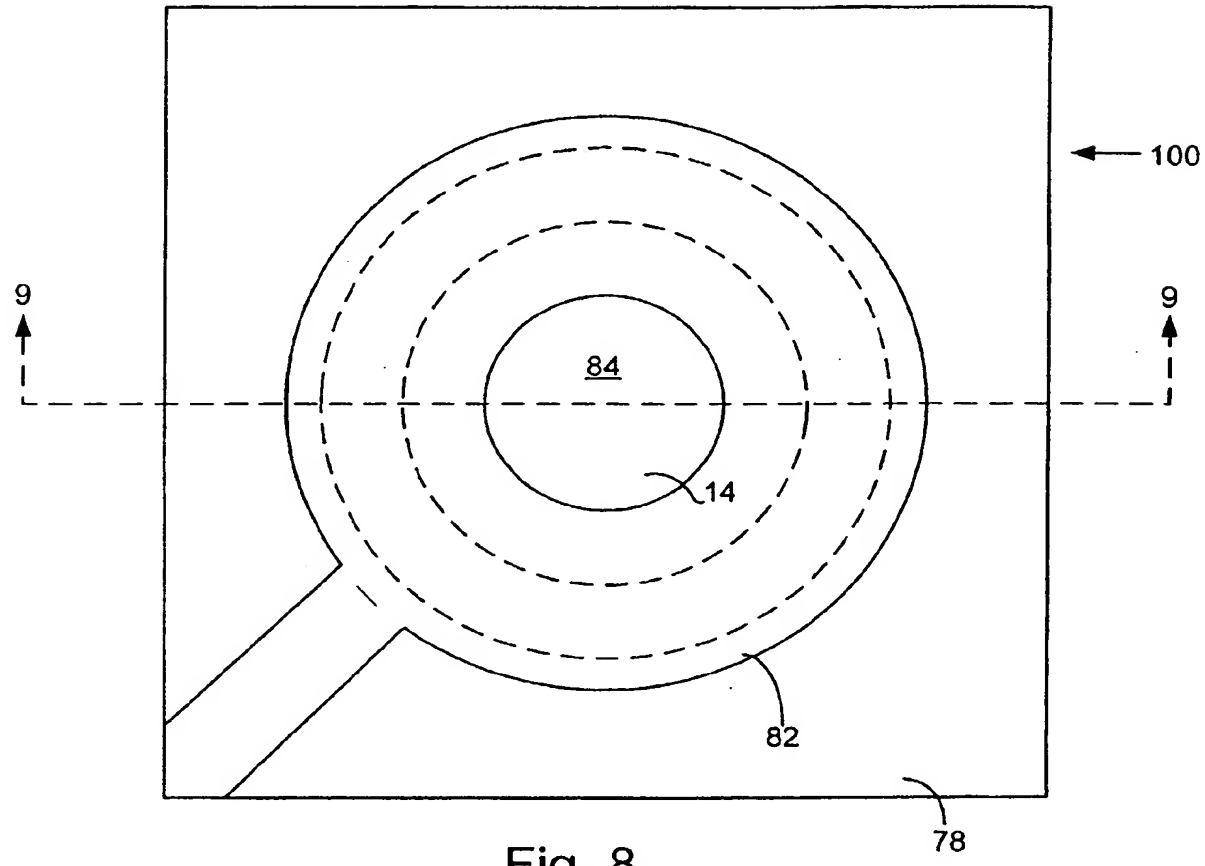

Fig. 8

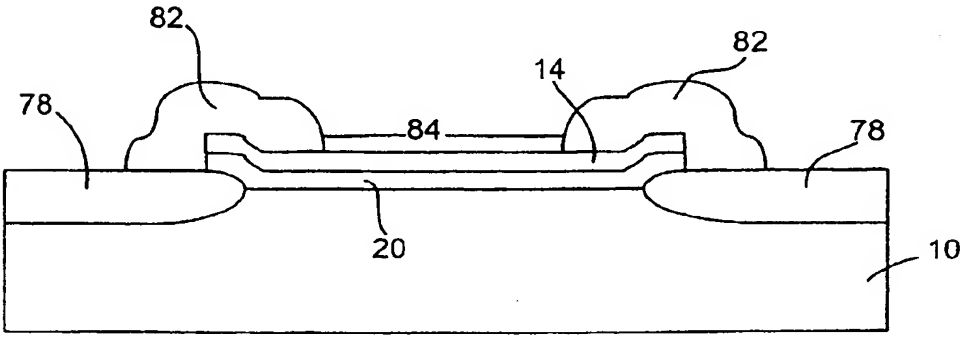

Fig. 9

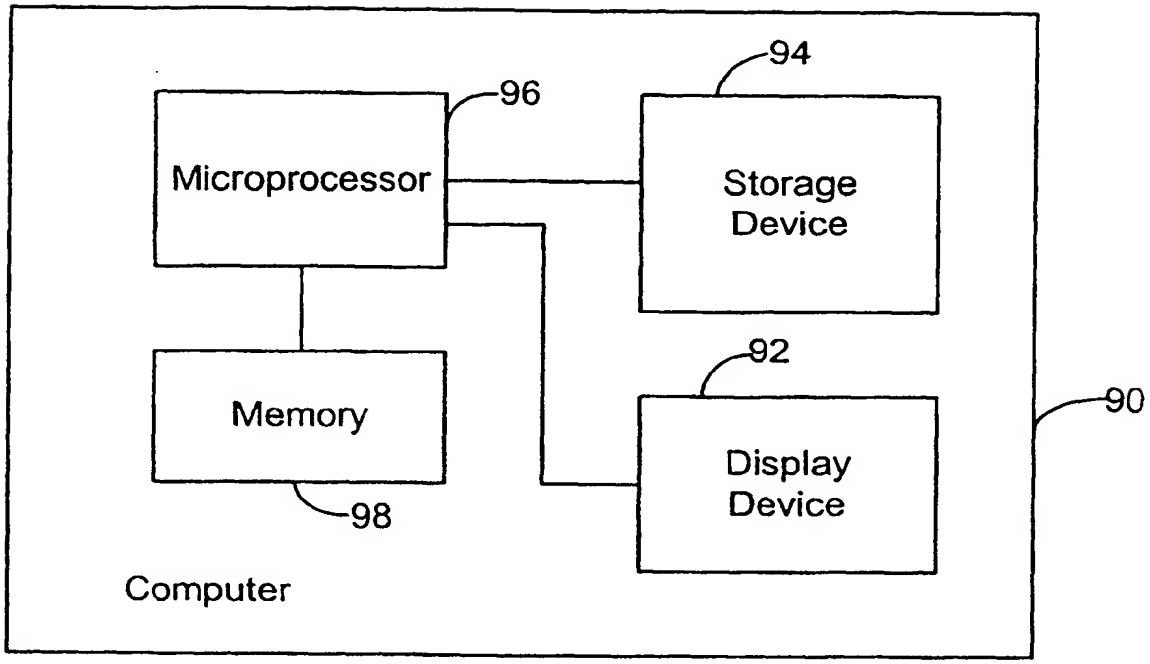

Fig. 10

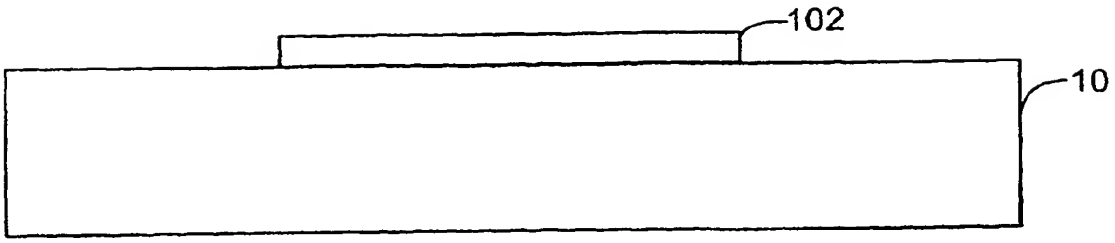

Fig. 11A

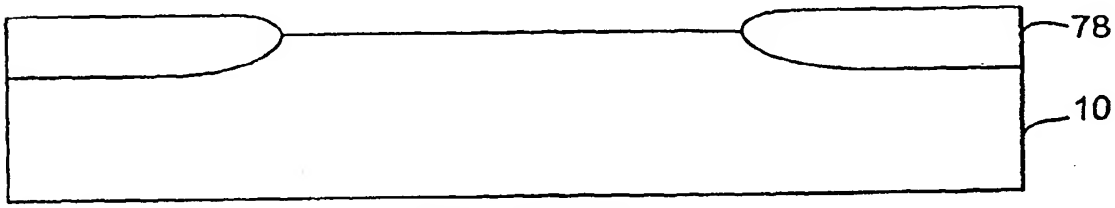

Fig. 11B

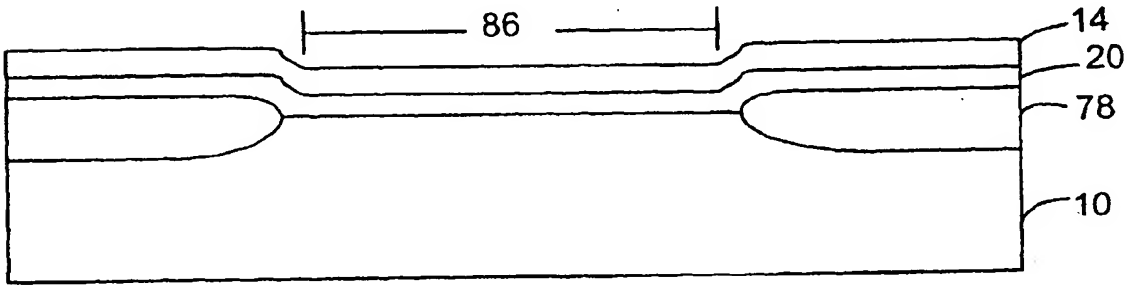

Fig. 11C

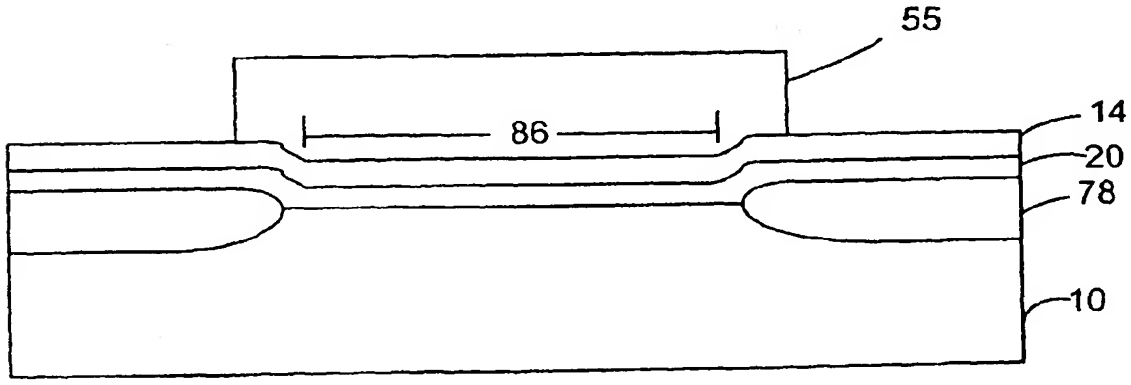

Fig. 11D

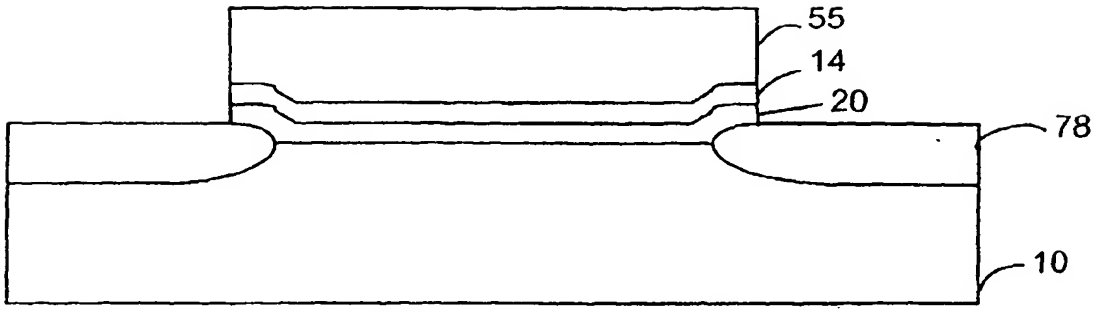

Fig. 11E

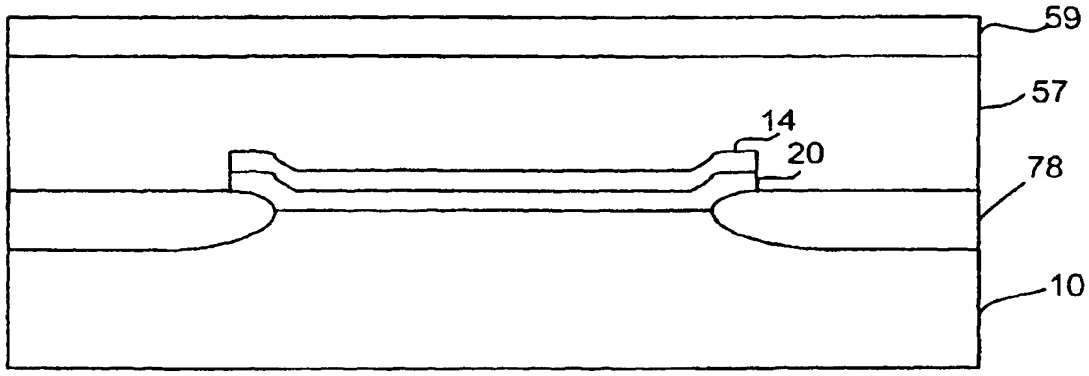

Fig. 11F

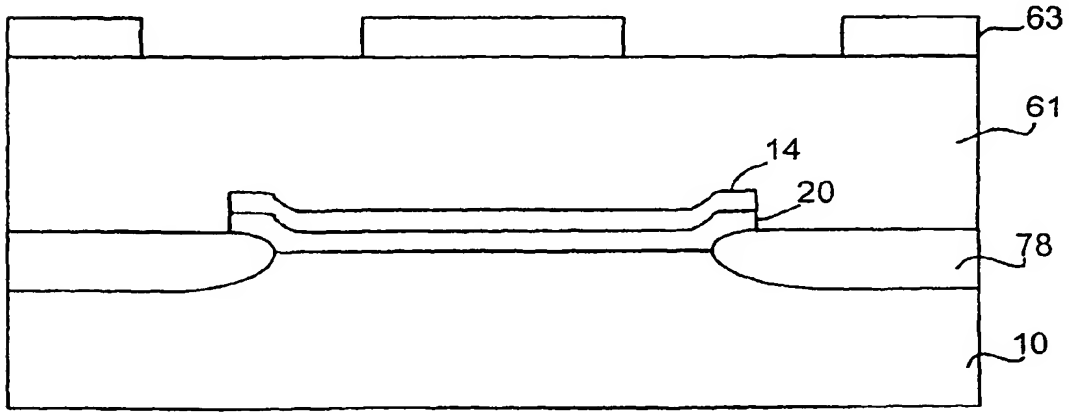

Fig. 11G

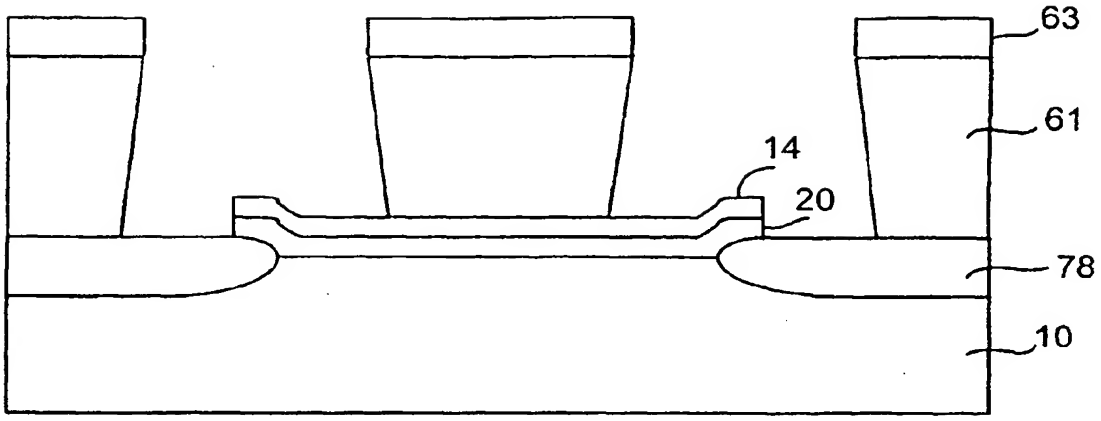

Fig. 11H

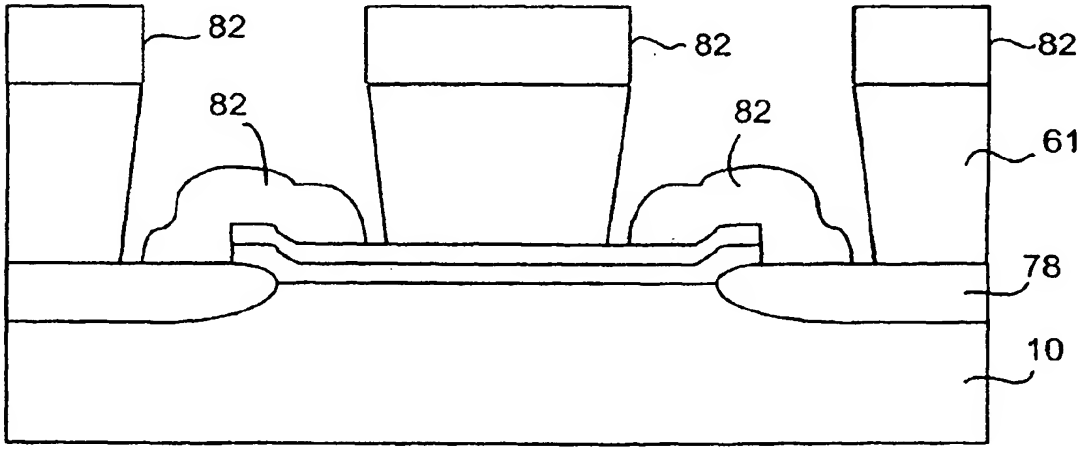

Fig. 11I

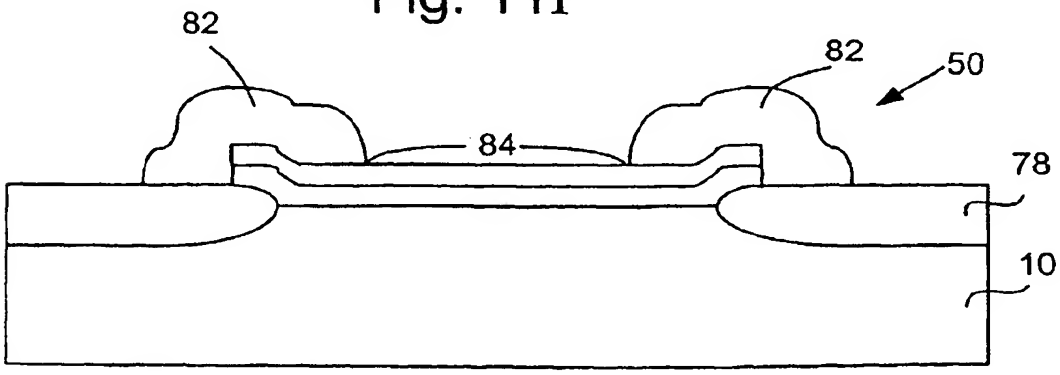

Fig. 11J

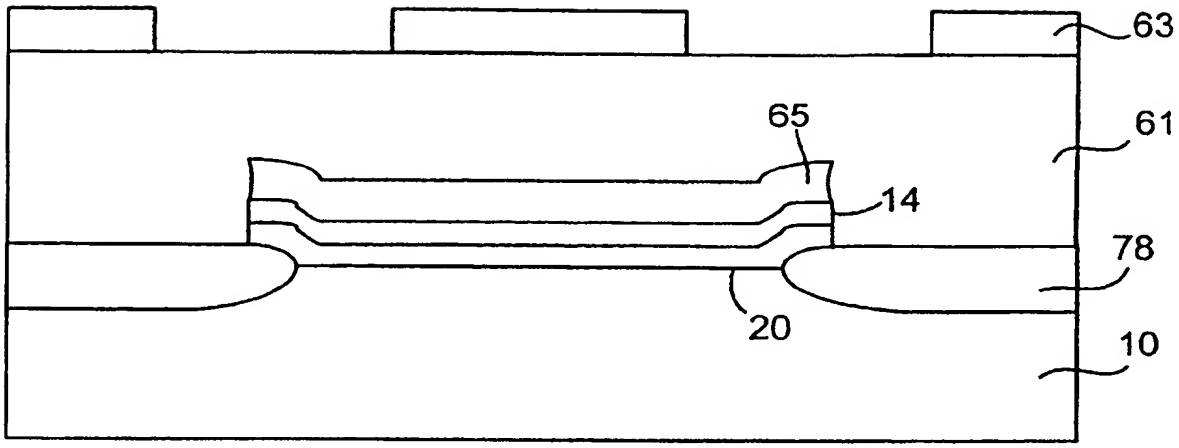

Fig. 12A

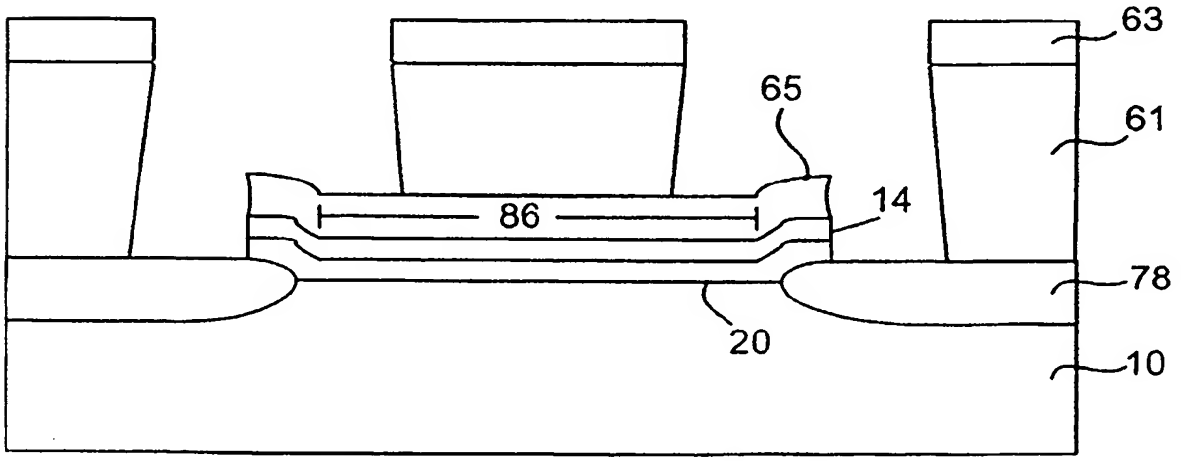

Fig. 12B

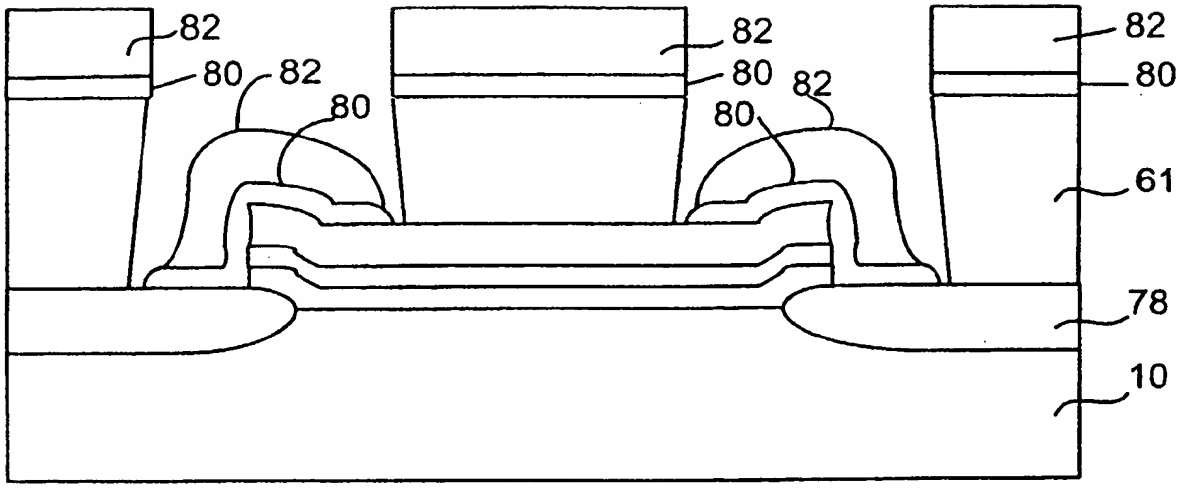

Fig. 12C

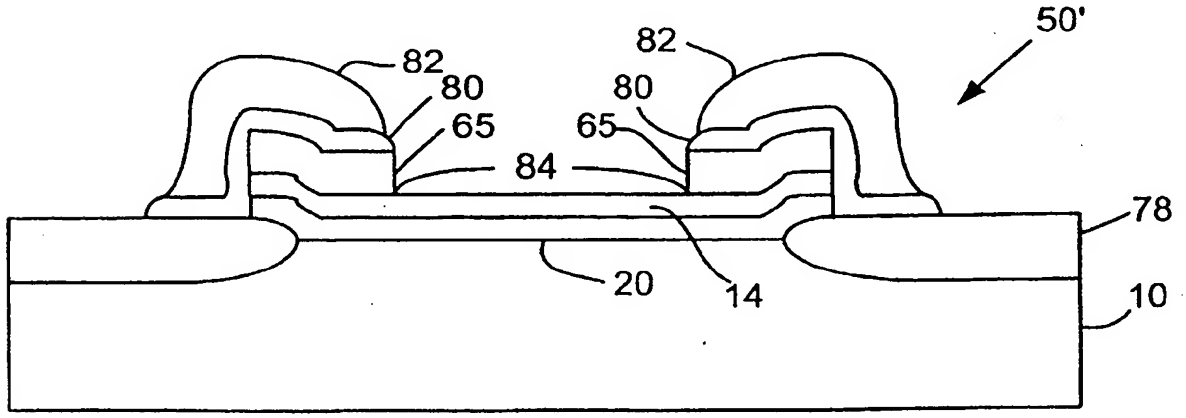

Fig. 12D

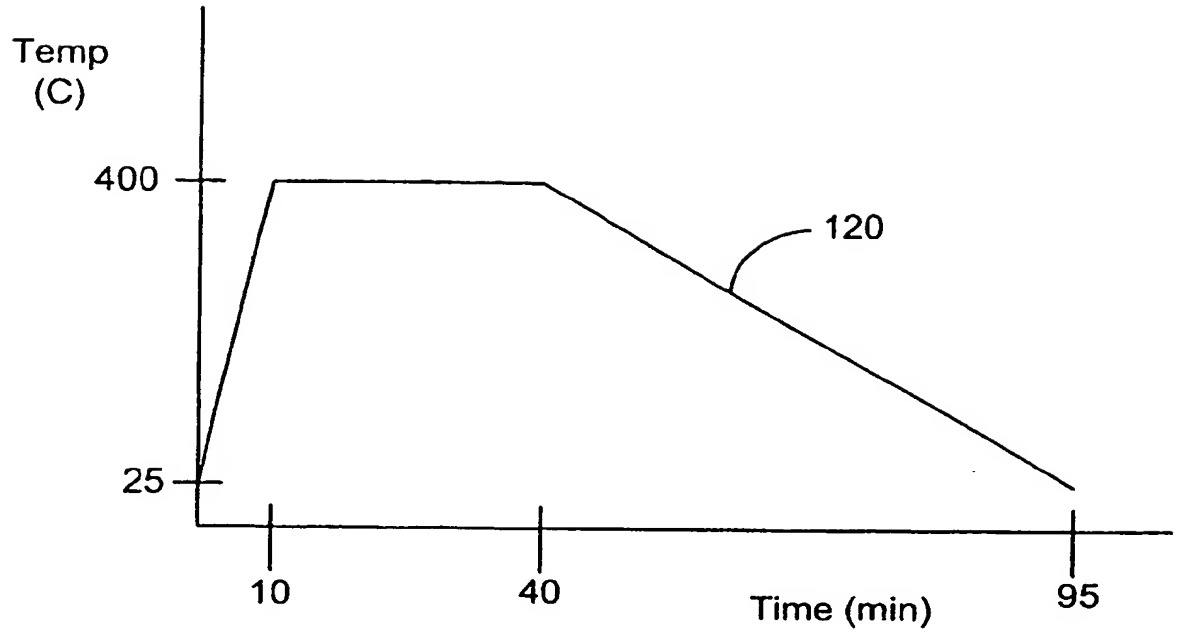

Fig. 13A

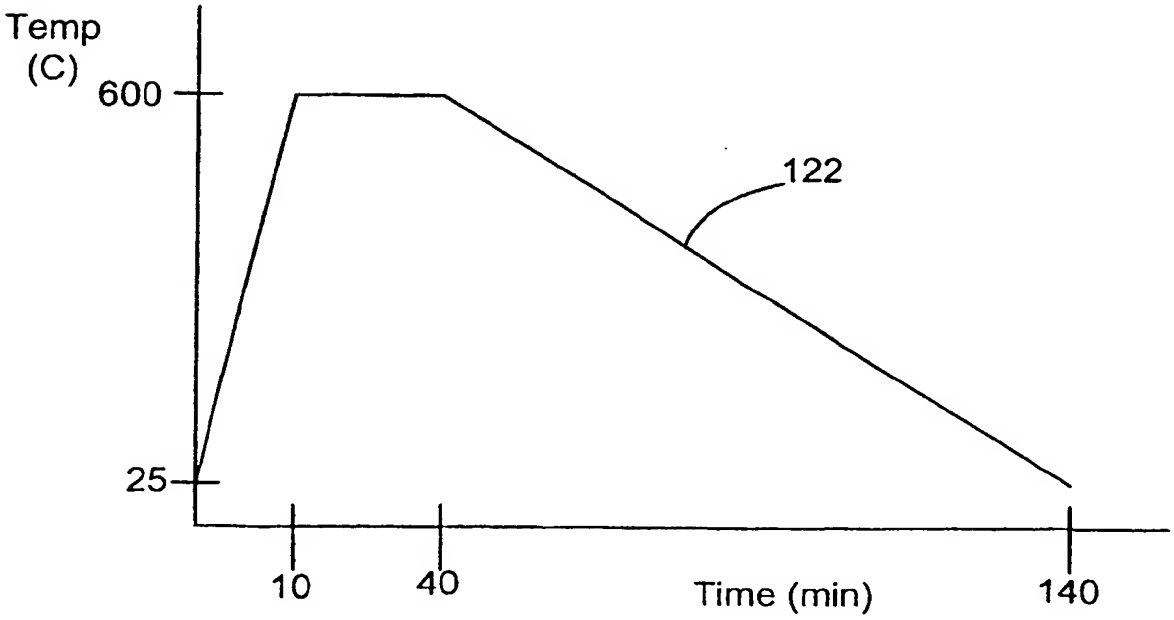

Fig. 13B